WHAT IS CLAIMED:

1. A post amplifier array implemented on an integrated circuit (IC) chip, the post amplifier array comprising:

a plurality of post amplifiers for receiving data signals, amplifying the received data signals, and outputting the amplified data signals, wherein the post amplifiers are capable of operating with multiple different input voltage levels.

2. The post amplifier array of claim 1, wherein the different input voltage levels are approximately 2.5V and 3.3V.

3. The post amplifier array of claim 1, further comprising:

said plurality of post amplifiers organized into first and second groups; and

a switch located between the second group of post amplifiers and an input power supply, wherein said first group of the post amplifiers is always electrically coupled to the input power supply to receive power during normal operation, and wherein the second group of post amplifiers are selectively electrically coupled to the input power supply to receive power only when the switch is turned on.

4. The post amplifier array of claim 3, wherein each of the first and second groups of post amplifiers is associated with overhead function circuitry, wherein the overhead circuitry associated with the first group always receives power during normal operation, and wherein the overhead circuitry associated with the second group receives power only when the switch is turned on.

5. The post amplifier array of claim 3, wherein the first group includes eight post amplifiers and the second group includes four post amplifiers.

6. The post amplifier array of claim 1, further comprising:

auto zero circuitry integrally connected to each individual post amplifier for performing an auto zero function of zeroing the dc component of the received data signals, wherein the auto zero circuitry does not require the use of an external capacitor to perform the auto zero function.

7. The post amplifier array of claim 6, wherein the auto zero circuitry includes a transistor, said transistor having a base, wherein leakage current from said base is used to perform the auto zero function.

8. The post amplifier array of claim 3, further comprising:

auto zero circuitry integrally connected to each individual post amplifier for performing an auto zero function of zeroing the dc component of the received data signals, wherein the auto zero circuitry does not require the use of an external capacitor to perform the auto zero function

9. The post amplifier array of claim 8, wherein the auto zero circuitry includes a transistor, said transistor having a base, wherein leakage current from said base is used to perform the auto zero function.

10. A post amplifier array implemented on an integrated circuit (IC) chip, thepost amplifier array comprising:

a plurality of individual post amplifiers, each post amplifier capable of receiving a data signal, amplifying the received data signal, and outputting the amplified data signal, the individual post amplifiers being organized into first and second groups; and

a switch located between the second group of post amplifiers and an input power supply, wherein said first group of the post amplifiers is always electrically coupled to the input power supply to receive power during normal operation, and wherein the second group of post amplifiers are selectively electrically coupled to the input power supply to receive power only when the switch is turned on.

11. The post amplifier array of claim 10, wherein each of the first and second groups of post amplifiers is associated with overhead function circuitry, wherein the overhead circuitry associated with the first group always receives power during normal operation, and wherein the overhead circuitry associated with the second group receives power only when the switch is turned on.

12. The post amplifier array of claim 10, wherein the first group includes eight post amplifiers and the second group includes four post amplifiers.

13. The post amplifier array of claim 10, wherein the post amplifiers are capable of

operating with multiple different input voltage levels.

14. The post amplifier array of claim 13, wherein the different input voltage levels are approximately 2.5V and 3.3V.

15. The post amplifier array of claim 10, further comprising:

auto zero circuitry integrally connected to each individual post amplifier for performing an auto zero function of zeroing the dc component of the received data signals, wherein the auto zero circuitry does not require the use of an external capacitor to perform the auto zero function.

16. The post amplifier array of claim 15, wherein the auto zero circuitry includes a transistor, said transistor having a base, wherein leakage current from said base is used to perform the auto zero function.

17. A post amplifier implemented on an integrated circuit (IC) chip, the post amplifier comprising:

input means for receiving data signals;

amplifying means for amplifying the received data signals;

output means for transmitting the amplified data signals; and

auto zero circuitry for performing an auto zero function of zeroing the dc component of the received data signals, wherein the auto zero circuitry does not require the use of an external capacitor to perform the auto zero function.

18. The post amplifier of claim 17, wherein the auto zero circuitry comprises a transistor, said transistor having a base, wherein leakage current from said base is used to perform the auto zero function.

19. The post amplifier of claim 17, wherein the post amplifier is capable of operating with multiple different input voltage levels.

20. The post amplifier of claim 17, wherein the different input voltage levels are approximately 2.5V and 3.3V.